Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 09-25-2007 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because the abstract is not a single paragraph on a separate sheet within the range of 50 to 150 words. Correction is required. See MPEP § 608.01(b).

5. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.

6. The disclosure is objected to because CROSS-REFERENCE TO RELATED APPLICATIONS are not listed and item (f) and (g) are not properly identified in the disclosure. Correction is required. See MPEP § 608.01.

Claim Objections

7. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 15-28 has been renumbered 14-27, since 1-13 claims are cancelled. The claim dependency also needs to be changed accordingly. Correction is required. See MPEP § 608.01.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 14, 15, 19, 20 and 22-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Boldt; Norton K. JR et al. (US 20060227085 A1).

Regarding Claim 14, Boldt; Norton K. JR et al. (US 20060227085 A1) discloses electrical circuit arrangement for a display device (page 3, paragraph 46), the electrical circuit arrangement comprising an input terminal for receiving a first signal (page 3, paragraph 46 suggests input signal received via electronic module and input terminal); a first memory element for storing information about the first signal (page 3, paragraph 46 suggests program memory stores the calibration value and shared memory stores first input signal); a driver element coupled to the first memory element for outputting a second signal via an output terminal in accordance with the information about the first signal (page 3, paragraph 46 suggests the electronic module provides adjusted PWM current to LED to display a image, please also see page 4, paragraph 56); a calibration circuit coupled between the driver element and the input terminal for matching a potential difference between the driver element and the input terminal during a calibration phase prior to receiving the first signal (page 4, paragraphs 51-55 suggests having a calibration circuitry to calibrate each pixel to required calibrated values), the matching

being such that there is no voltage change required at the input terminal during a subsequent programming phase if during this programming phase the second signal has to be programmed to the same value as during the previous programming phase (page 5 and 6, paragraphs 61-70 suggests the if any degradation occurred between input phase and output phase the LEDs are calibrated to and the amount of energy or voltage required to bring the output to the original level; if there is no degradation from input to output terminal the calibration process is avoided and the programming phase assigns same value as during the previous programming phase, please also see page 6, paragraphs 75-78).

Regarding Claim 15, Boldt; Norton K. JR et al. (US 20060227085 A1) discloses the calibration circuit comprising a calibration switch for coupling the input terminal to a calibration voltage (please see pages 5 and 6 paragraphs 61-70 and 75-78).

Regarding Claim 19, Boldt; Norton K. JR et al. (US 20060227085 A1) discloses a further switch coupled between the driver element and the output terminal (please see figures 2, 12 and 13 and pages 5 and 6, paragraphs 61-70, 75-78).

Regarding Claim 20, Boldt; Norton K. JR et al. (US 20060227085 A1) discloses a switch coupled between the driver element and the calibration circuit (please see figures 2, 12 and 13 and pages 5 and 6, paragraphs 61-70, 75-78).

Regarding Claim 22, Boldt; Norton K. JR et al. (US 20060227085 A1) discloses first memory element comprises a capacitor (please see figures 2, 12 and 13 and pages 5 and 6, paragraphs 61-70, 75-78).

Regarding Claim 23, Boldt; Norton K. JR et al. (US 20060227085 A1) discloses Display device comprising a plurality of display pixels (please see figure 13, page 2, paragraph 24), the display pixels comprising an electrical circuit arrangement (page 3, paragraph 46), and an emissive element coupled to said output terminal and adapted to emit light on reception of said second signal (pages 3 and 4, paragraph 46-56); and a display controller adapted to control the calibration phase of the plurality of display pixels (pages 5 and 6, paragraphs 61-70, 75-78).

Regarding Claim 24, Boldt; Norton K. JR et al. (US 20060227085 A1) discloses each input terminal one common calibration switch for coupling the input terminal to a calibration voltage (please see figures 2, 12, 13 and pages 5 and 6, paragraphs 61-70, 75-78).

Regarding Claim 25, Boldt; Norton K. JR et al. (US 20060227085 A1) discloses signal-processing circuitry for supplying an input signal to a data input of the display controller (please see figures 2, 12, 13 and pages 5 and 6, paragraphs 61-70, 75-78).

Regarding Claim 26, Boldt; Norton K. JR et al. (US 20060227085 A1) discloses each of said arrangements being adapted to receive a data signal as said first signal and to output said

second signal to a column electrode coupled to a plurality of display pixels along said column electrode (please see figures 2, 12, 13 and pages 5 and 6, paragraphs 61-70, 75-78).

Regarding Claim 27, Boldt; Norton K. JR et al. (US 20060227085 A1) discloses Method for addressing a display pixel of a display device comprising an input terminal (page 2, paragraph 24, pages 3 and 4, paragraphs 46-56), a first memory element, a second memory element, a driver transistor coupled to an output terminal (please see figures 2, 12, 13 and pages 5 and 6, paragraphs 61-70), and a calibration circuit coupled between the driver transistor and the input terminal (please see figures 2, 12, 13 and pages 5 and 6, paragraphs 61-70, 75-78), the method comprising the steps of: a first memory element for storing information about the first signal (page 3, paragraph 46 suggests program memory stores the calibration value and shared memory stores first input signal); a driver element coupled to the first memory element for outputting a second signal via an output terminal in accordance with the information about the first signal (page 3, paragraph 46 suggests the electronic module provides adjusted PWM current to LED to display a image, please also see page 4, paragraph 56); a calibration circuit coupled between the driver element and the input terminal for matching a potential difference between the driver element and the input terminal during a calibration phase prior to receiving the first signal (page 4, paragraphs 51-55 suggests having a calibration circuitry to calibrate each pixel to required calibrated values), the matching being such that there is no voltage change required at the input terminal during a subsequent programming phase if during this programming phase the second signal has to be programmed to the same value as during the previous programming phase (page 5 and 6, paragraphs 61-70 suggests the if any degradation occurred between input

phase and output phase the LEDs are calibrated to and the amount of energy or voltage required to bring the output to the original level; if there is no degradation from input to output terminal the calibration process is avoided and the programming phase assigns same value as during the previous programming phase, please also see page 6, paragraphs 75-78).

Allowable Subject Matter

10. Claims 16-18 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Olivier F. Parche (US 2002/0044110 A1) Grayscale static pixel cell for OLED active matrix display.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PRABODH M. DHARIA whose telephone number is (571)272-7668. The examiner can normally be reached on M-F 8-30AM to 5PM.

13. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

/Prabodh M Dharia/

Primary Examiner

Art Unit 2629

January 05, 2010